

## Abstract

A semiconductor device having a chip-on-chip structure wherein; a first semiconductor chip with a memory macro control circuit where a plurality of inter-chip connection terminals and a plurality of external connection terminals are formed on a surface of the chip; and a second semiconductor chip with memory macro having input/output terminals for the normal operation mode and for the test mode where a plurality of inter-chip connection terminals and a plurality of external connection terminals are formed on a surface of the chip; are adhered to each other in a form so that the surfaces of the chips are opposed to each other and so that the inter-chip connection terminals of the first semiconductor chip and the inter-chip connection terminals of the second semiconductor chip are connected to each other; is provided wherein a multiplexer circuit and a demultiplexer circuit are provided with the first semiconductor chip and the second semiconductor chip so that a signal is inputted to, or is outputted from, the memory macro via the common inter-chip connection terminals by switching signal transmission channels in either case, during normal operation mode or during memory macro test mode which is carried out after the connection of the chips.